**CHAPTER 1**

**INTRODUCTION**

**1.1 Background of the Study**

One of the most important sensory ability of humans with the highest information density is vision.[2] The filtration methods of the human scene understanding capability is able to operate even in the high abundance of information by focusing on some elements while suppressing the rest. Artificial visual attention has been one of the key methodologies taken from nature that inspire researchers to develop robust and efficient machine vision systems for visual search applications.

As a scientific discipline Computer Vision collects the theory for building artificial systems that obtain information from images. Image data can either be a video frame, view from multiple cameras, or a multi-dimensional data from a medical scanner. Modern computer vision systems are applied in fields of process control, event detection, information organization, modeling of objects and man-machine interaction. The mentioned applications are often found applied in a wide array of industrial commercial, home and office applications. [1]

The study of computer vision describes the artificial vision system implemented in either software or hardware or the combination of both. One such software implementation is the open source computer vision library more commonly called as OpenCV. This library of programming function mainly aimed at real-time computer vision is free for use under the Berkeley Software (BSD) license. Released around 1999, OpenCV was a project from an Intel Research initiative to advance CPU-intensive applications. [1]

In this study the researcher will focus on investigating the potential of Altera’s Cyclone V System on a Chip (SoC) with built in ARM Hard Processor component and FPGA Fabric for the application of Face Detection using the Open Source Computer Vision Library OpenCV. The SoCKit Development board will be used as the hardware platform for this study. The study will initially go through Development of the SoC Hardware and Software Integration, adaption of the Linux Operating System for running on the CycloneV SoC, and the compilation and to Integrate OpenCV for a Face Detection System utilizing the SoC.

**1.2 Statement of the Problem**

This paper had aimed to develop an Integrated Face Detection system using the OpenCV Library that operates on the CycloneV ARM and FPGA SoC Development Board called SoCKit.

**1.3 Objectives of the Study**

The general objectives of this study were:

1. developed the Hardware and Software Integration system required to run Linux on the CycloneV SoC SoCKit Development Board;
2. developed a custom version of the Linux Open Source Operating System that will be compatible with the system CycloneV SoC SoCKit Development Board;
3. compiled and installed the OpenCV library on to the Linux System;
4. integrated the Face Detection System using the Installed OpenCV Library with the rest of the subsystems;
5. and compared the performance parameters of the Face Detection system on an CISC Intel based platform.

**1.4 Significance of the Study**

This study aims to develop solutions for allowing the OpenCV Library to run on a Hybrid ARM and FPGA hardware. This will open opportunities for future research on accelerated performance of the OpenCV library for computer vision on ARM based devices using the FPGA fabric of the Cyclone V SoC. Considering the wide array of industries OpenCV is currently being implemented, and the prevalence of ARM on commercial and industrial applications, the future potential acceleration will provide a more efficient and scalable use of the OpenCV library in different fields of its application by different industries.

**1.5 Scope and Limitations**

In this study:

1. only the SoCKit Cyclone V Development Board was used for the prototype;
2. for the software and hardware integration, in order to reduce code complexity and build time to reasonable levels, only the necessary hardware components required for the research was integrated in to the system;
3. only a selected number of Linux Operating System subsystems was adopted to run on the SoCKit Cyclone V Development Board;
4. and to reduce cost, the primary image input method was through USB Video Class support which was compatible only with limited models of off-the-shelf USB Web Cameras. For this study, the Logitech C525 Camera was used.

**1.6 Definition of Terms**

**ARM Architecture** - is a family of instruction set architectures for computer processors based on a reduced instruction set computing (RISC) architecture developed by British company ARM Holdings.[7]

**Complex Instruction Set Computer** (CISC) - is a computer where single instructions can execute several low-level operations (such as a load from memory, an arithmetic operation, and a memory store) and/or are capable of multi-step operations or addressing modes within single instructions.[9]

**Development Board** - A microprocessor development board is a printed circuit board containing a microprocessor and the minimal support logic needed for an engineer to become acquainted with the microprocessor on the board and to learn to program it.[16]

**Direct memory access (DMA)** - Is a feature of modern computers that allows certain hardware subsystems within the computer to access system memory independently of the central processing unit (CPU). [4]

**Ethernet** - is a family of computer networking technologies for local area networks (LANs).[12]

**Field-Programmable Gate Array** (FPGA) - is an integrated circuit designed to be configured by a customer or a designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). [5]

**IP Core -** In electronic design a semiconductor intellectual property core, IP core, or IP block is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party. IP cores may be licensed to another party or can be owned and used by a single party alone. The term is derived from the licensing of the patent and/or source code copyright that exist in the design. IP cores can be used as building blocks within ASIC chip designs or FPGA logic designs. [20]

**Network on chip (NoC)** - is a communication subsystem on an integrated circuit (commonly called a "chip"), typically between IP cores in a system on a chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. NoC technology applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs. [21]

**PHY** - An instantiation of PHY connects a link layer device (often called MAC as an abbreviation for Media Access Control) to a physical medium such as an optical fiber or copper cable. A PHY device typically includes a Physical Coding Sub layer (PCS) and a Physical Medium Dependent (PMD) layer.[18]

**Pixels** - a physical point in a raster image, or the smallest addressable element in an all points addressable display device; so it is the smallest controllable element of a picture represented on the screen. [15]

**Processor** - is the hardware within a computer that carries out the instructions of a computer program by performing the basic arithmetical, logical, and input/output operations of the system.[6]

**Reduced Instruction Set Computing** (RISC) - is a CPU design strategy based on the insight that simplified (as opposed to complex) instructions can provide higher performance if this simplicity enables much faster execution of each instruction.[8]

**System on a Chip (SOC)** - A system on a chip or system on chip (SoC or SOC) is an integrated circuit (IC) that integrates all components of a computer or other electronic system into a single chip. [3]

**ULPI** - is an interface standard for high-speed USB 2.0 IP systems. It defines an interface between USB IP link controllers (such as MUSBHDRC) and the PHYs or transceivers that drive the actual bus. ULPI stands for UTMI+ low pin interface and is designed specifically to reduce the pin count of discrete high-speed USB PHYs.[17]

**Universal Serial Bus** (USB) - is an industry standard developed in the mid-1990s that defines the cables, connectors and communications protocols used in a bus for connection, communication, and power supply between computers and electronic devices.[13]

**Unshielded twisted pair** (UTP) - cables are found in many Ethernet networks and telephone systems.[19]

**USB On-The-Go** (USB OTG) - is a specification that allows USB devices such as digital audio players or mobile phones to act as a host, allowing other USB devices like a USB flash drive, digital camera, mouse, or keyboard to be attached to them. Unlike conventional USB systems, USB OTG systems can drop the hosting role and act as normal USB devices when attached to another host. This can be used to allow a mobile phone to act as host for a flash drive and read its contents, downloading music for instance, but then act as a flash drive when plugged into a host computer and allow the host to read data from the device. [14]

**Video Graphics Array** (VGA) - refers specifically to the display hardware first introduced with the IBM PS/2 line of computers in 1987, but through its widespread adoption has also come to mean either an analog computer display standard, the 15-pin D-subminiature VGA connector or the 640x480 resolution itself. Today, the VGA analog interface is used for high definition video including 1080p and higher. While the VGA transmission bandwidth is high enough to support even higher resolution playback, there can be picture quality degradation depending on cable quality and length.[10]

**Webcam** - A webcam is a video camera that feeds its image in real time to a computer or computer network. Unlike an IP camera (which uses a direct connection using Ethernet or Wi-Fi), a webcam is generally connected by a USB cable, FireWire cable, or similar cable.[11]

**1.7 Theoretical Framework**

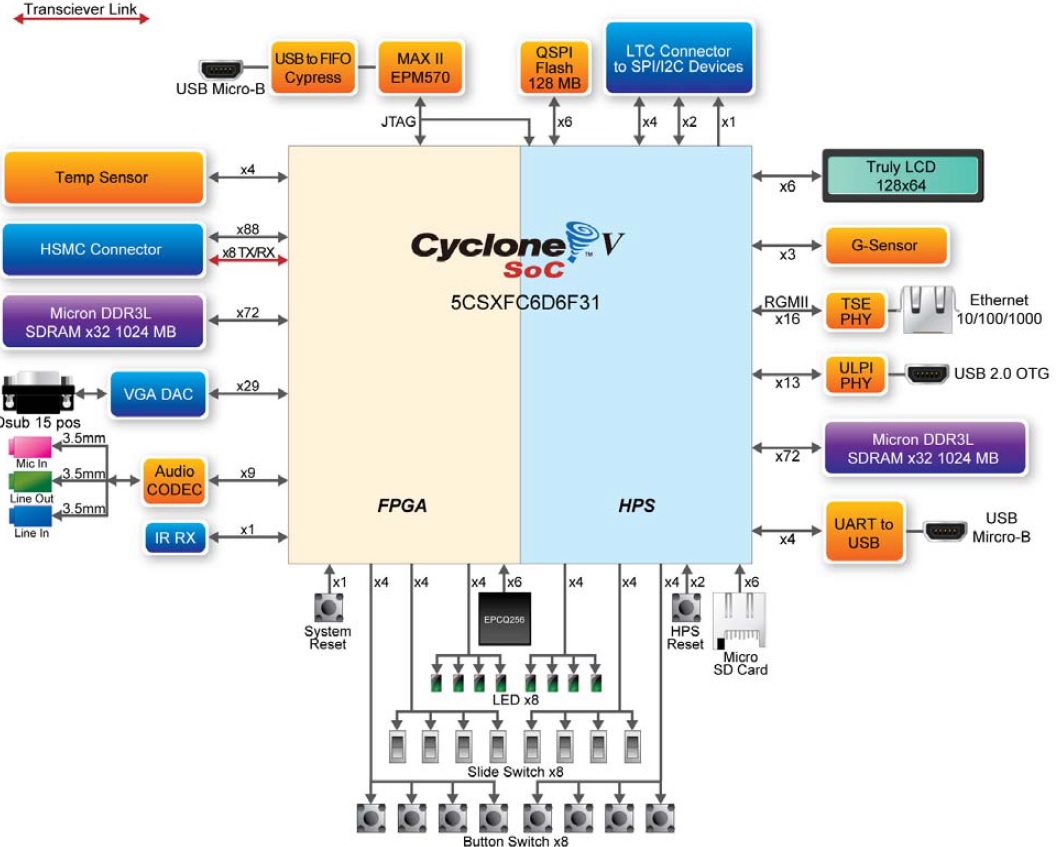
**1.7.1 Hardware**

This study requires the use of the SoCKit Evaluation Board and its on-board peripherals. In this section the components, their relevance to the study and associated technical data are introduced.

**1.7.1.1 SoCKit Development Board**

The board combines Cortex-A9 embedded cores with the FPGA fabric using a high-bandwidth interconnect backbone. Specifically, it contains Altera Cyclone V SoC with Dual ARM® Cortex®-A9 processors and 110K Les, High Speed Mezzanine Connector (HSMC) including transceivers, two banks of low-power DDR3 memory a MicroSD card and Ethernet 10/100/1000 interfaces, Adjustable clock output by Silicon Labs, Graphic LCD: 128 x 64 (SPI Interface), VGA and Audio connections, USB 2.0 OTG (Full Speed) and USB to UART connections with 3-Axis digital accelerometer and temperature sensor. [22]

Of particular interest in this study is the Cyclone V SoC inside the Development board, the board’s USB OTG interface Support, VGA interface Support, Memory ICs and Ethernet interface support. Refer to Appendix B for the complete specification of the SoCKit Evaluation Board. The **Figure 1** below shows the system block diagram of the SoCKit Evaluation Board.

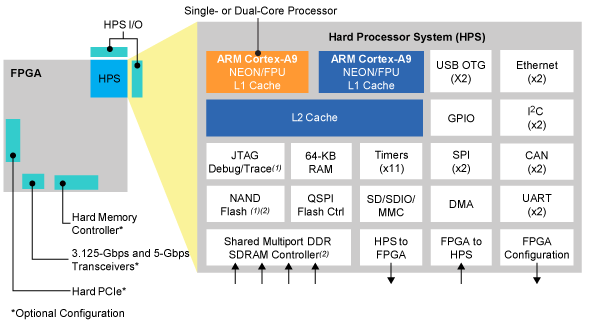


**Figure 1.** System Block Diagram of the SoCKit Evaluation Board

**1.7.1.1.1 Cyclone V SoC**

Quoted from the Altera Website, “the Altera SoCs integrate an ARM-based hard processor system (HPS) consisting of processor, peripherals, and memory interfaces with the FPGA fabric using a high-bandwidth interconnect backbone. The Cyclone® V SoCs reduce system power, system cost, and board size while increasing system performance by integrating discrete processor, FPGA, and digital signal processing (DSP) functions into a single, user customizable ARM-based system on a chip (SoC)”. [23]

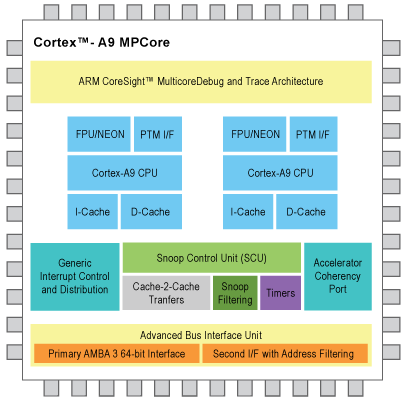
For this Study a number of selected subsystems of the Cyclone V SoC will be used to develop the Face Detection System. Shown below is the block diagram of the Cyclone V SoC integrated circuit. Shown in **Figure 2** is the Cyclone V IC (Integrated Circuit) Block Diagram.



**Figure 2.** Cyclone V SoC Integrated Circuit Block Diagram

It features a 925 MHz, dual-core ARM® Cortex™-A9 MPCore™ processor with each processor having 32 KB of L1 instruction cache, 32 KB of L1 data cache, Single- and double-precision floating-point unit and NEONTM media engine, CoreSightTM debug and trace technology. And of particular interest, the IC also contains Multiport SDRAM controller with support for DDR2, DDR3, and LPDDR2 and optional error correction code (ECC) support, SD/SDIO/MMC controller with DMA, 2x 10/100/1000 Ethernet media access control (MAC) with DMA, and 2x USB On-The-Go (OTG) controller with DMA. [23]

**1.7.1.1.1.1 Dual-Core ARM Cortex-A9 MPCore Processor**

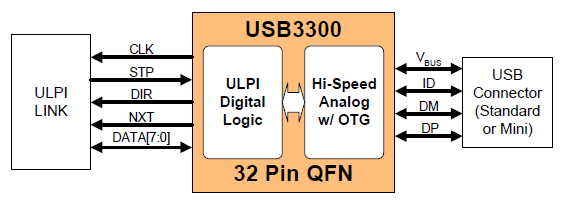


**Figure 3.** Cortex A9 MPCore

The ARM Cortex-A9 processor with its Block Diagram shown in **Figure 3** is combined with a rich set of embedded peripherals, interfaces, and on-chip memories to create a complete hard processor system (HPS). The high-bandwidth on-chip backbone connecting the HPS and FPGA fabric provides over 100 Gbps peak bandwidth, ideal for sharing data between the ARM processor and hardware accelerators within the FPGA fabric. Full specification listing is available on **Appendix C** as listed on the ARM Cortex Portion of the Altera Company Website.[24]

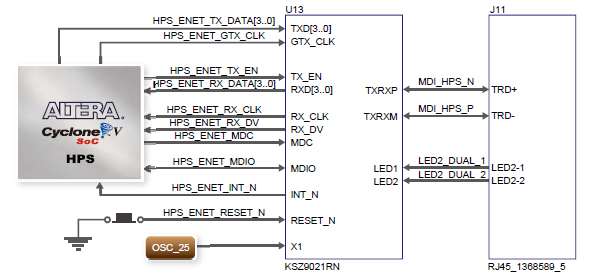
**1.7.1.1.2 USB 3300 Hi-Speed USB Host, Device or OTG PHY**

The built-in USB Controller shown in **Figure 4** of the board is the SMSC USB3300 Hi Speed USB Host, Device or OTG PHY with ULPI Low Pin Interface. It supports USB Specification Rev 2.0. In addition it supports OTG Monitoring of VBUS levels with internal comparators. This controller will become the input interface of the shelf USB Webcam to be used for the input image of the Face Detection system. [25]



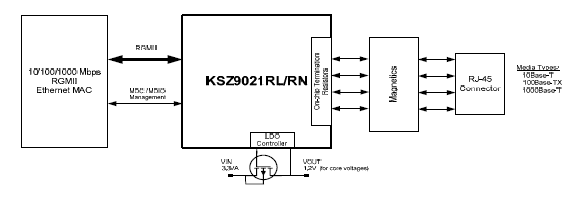
**Figure 4.** Basic ULPI USB Device Block Diagram

**1.7.1.1.3 KSZ9021RL/RN Gigabit Ethernet Transceiver**



**Figure 5.** Connections between Cyclone V SOC and FPGA and Ethernet

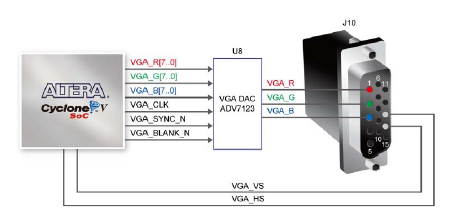
The KSZ9021RL/RN is a completely integrated triple speed Ethernet Physical Layer Transceiver for transmission and reception of Data over standard CAT-5 unshielded twisted pair (UTP) cable. This subsystem is of particular interest to this research because it will be used as the Network Connection in download, compilation and installation of important Linux, OpenCV and other Software’s Source Code and Associated Libraries. **Figure 6** shows the Functional Block Diagram of the Ethernet PHY and **Figure 5** shows the Connections between FPGA and Ethernet. [26]



**Figure 6.** Functional Block Diagram of the KSZ9021RL/RN

**1.7.1.1.4 VGA**

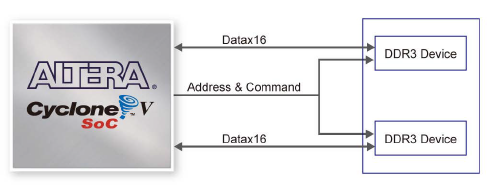
The board includes a 15-pin D-SUB connector for VGA output. The VGA synchronization signals are provided directly from the Cyclone V SoC FPGA, and the Analog Devices ADV7123 triple 10-bit high-speed video DAC (only the higher 8-bits are used) is used to produce the analog data signals (red, green, and blue). It could support the SXGA standard (1280\*1024) with a bandwidth of 100MHz. **Figure 7** shows the associated block Diagram. The VGA will be the interface used to connect the FPGA to the Display Monitor for display of output. [27]



**Figure 7.** VGA Block Diagram

**1.7.1.1.5 Memory**

The board supports 1GB of DDR3 SDRAM comprising of two x16 bit DDR3 devices on FPGA side. The DDR3 devices shipped with this board are running at 400MHz if the hard external memory interface is enabled, and at 300MHz if the hard external memory interface if not enabled. **Figure 8** shows the connections between the DDR3 and Cyclone V SoC FPGA. The HPS memory must be considered during the system integration phase of the system. [27]



**Figure 8.** Connections between FPGA and DDR3

**1.7.1.2 Logitech C525 Webcam**

For the image input, an off the shelf USB Web Cam will be utilized. For this research the Logitech C525 Webcam is the model to be used. The Logitech C525 is capable of up to 1280 x 720 pixels for video resolutions and has 8 megapixels for still images. In addition, the researcher also intends to use this as a Mouse and Keyboard interface in conjunction with the Synergy Open Source Virtual KVM Software. [28]

**1.7.1.3 Micro SD Card**

The Micro Secure Digital (SD) is a non-volatile memory card format for use in portable devices, such as mobile phones, digital cameras, GPS navigation devices, and tablet computers. This Memory Card acts as the NAND Flash Memory for the Linux Operating System Files, and Device Tree structure. [29]

**1.7.2 Software**

In this paper two sets of categories for software will be made. First is the In-System software will be the software to be included inside the System in development. The second category will be the Development Software which will be software used in the development of the System.

**1.7.2.1 In-System**

Subsystems found inside the System being developed is referred to as In-System Software in this document. Some of the relevant In-System components, their relevance to the study and their technical details are discussed in this section.

**1.7.2.1.1 Linux Kernel**

The Linux Kernel will be the main Kernel used for the Linux Operating System to be deployed in the CycloneV SoC. The Linux kernel is a Unix-like operating system kernel used by a variety of operating systems based on it, which are usually in the form of Linux distributions. The Linux kernel is released under the GNU General Public License version 2 (GPLv2) (plus some firmware images with various non-free licenses), and is developed by contributors worldwide. [30]

**1.7.2.1.2 Debian Operating System**

Debian will be the operating System used in conjunction with the Linux Kernel. It is composed of free software mostly carrying the GNU General Public License. The operating system is developed by an internet collaboration of volunteers aligned with The Debian Project. On top of Debian is where the OpenCV Library will be installed.

**1.7.2.1.3 OpenCV Library**

OpenCV (Open Source Computer Vision Library) is a library of programming functions mainly aimed at real-time computer vision, developed by Intel, and now supported by Willow Garage and Itseez. It is free for use under the open source BSD license. The library is cross-platform. It focuses mainly on real-time image processing. The OpenCV libraries functions and modules will be used for the development of the Face Detection System for the Altera Cyclone V Development Board. [1]

**1.7.2.1.4 Lightweight X11 Desktop Environment (LXDE)**

The project utilizes the LXDE for the Modified Debian Based Linux Operating System. LXDE is an energy saving and extremely fast performing desktop solution. It works well with computers on the low end of the performance spectrum such as new generation netbooks and other small mobile computers. LXDE is designed for cloud networks such as local freifunk clouds or the global Internet cloud. It can be built on top of various Linux distributions such as Ubuntu, Debian or Fedora. It supports a wealth of programs that can be installed with Linux systems locally. LXDE already supports many computer processor architectures including Intel, MIPS and ARM. In this case, we’re using the LXDE ARM support for processor compatibility. [32]

**1.7.2.2 Development Software**

**1.7.2.2.1 Altera Quartus**

In order to design and compile the Hardware Description Code and IP Blocks of the System, the Altera Quartus II Complete Design Suite is used. Quartus II is a software tool produced by Altera for analysis and synthesis of HDL designs, which enables the developer to compile their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. The version utilized for this project is 13sp1 which is a service pack of version 13. [33]

**1.7.2.2.2 Qsys - Altera’s System Integration Tool**

The researcher also made use of the Qsys system integration for the FPGA design process by automatically generating interconnect logic to connect intellectual property (IP) functions and subsystems. Qsys is the next-generation SOPC Builder tool powered by a new FPGA-optimized network-on-a-chip (NoC) technology delivering higher performance, improved design reuse, and faster verification compared to SOPC Builder. [34]

**1.7.2.2.3 SoC Embedded Design Suite**

The SoC EDS is a comprehensive tool suite for embedded software development on Altera SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems. The SoC EDS includes an exclusive offering of the ARM Development Studio™ 5 (DS-5™) Altera Edition Toolkit. The SoC EDS is used by the researcher to compile and use pre-built U-Boot and Linux build environments. [35]

**1.7.2.2.4 Linaro Toolchain**

The Linaro Toolchain is maintained by the Linaro Toolchain Working Group. The Linaro Toolchain deals with aspects of system-level tools - the core development toolchain compiler, assembler, linker, debugger, emulation, profiling and analysis using oprofile, and performance events and instrumentation with ftrace. Of particular interest in this research is the Linaro GCC Tool Chain. [36]

**1.7.2.2.4.1 Linaro GCC**

The GNU Compiler Collection (GCC) is a compiler system produced by the GNU Project supporting various programming languages. GCC is a key component of the GNU toolchain. The Free Software Foundation (FSF) distributes GCC under the GNU General Public License (GNU GPL). Linaro GCC is a fork of the GNU GCC, and is a performance focused branch of the current GCC stable release and includes back ports of the improvements and bug fixes that Linaro and others have done upstream. The researcher used the Linaro GCC in compiling ported code for both the Linux Kernel, and the Linux Kernel Modules. [37]

**1.7.2.2.5 Github**

Github is not a software per se but a web-based hosting service for software development projects that use the Git revision control system. This research has a heavy use of this web service due to complexities in managing software versioning and the wide array of libraries, software, and configuration files necessary for this project. The real software behind it is Git. Git is a free and open source distributed version control system designed to handle everything from small to very large projects with speed and efficiency. [38]

**1.7.2.2.6 Win32 Disk Imager**

This is a Windows program for saving and restoring images from removable drives (USB drives, SD Memory cards, etc). It can be used to write boot images (i.e. ubuntu-12.04-preinstalled-desktop-armhf+omap4.img) to a SD Flash device or USB flash device, making it bootable. It currently does not support writing an ISO image to USB. The researcher has a heavy use of this software to backup and restore images that are compiled using the Linaro Tool Chain. Compilation and reconfiguration takes a huge amount of time in the development process and this tool is most helpful in making sure data are saved on the PC and restored to the MicroSD Cards. [39]

**1.7.2.2.7 PuTTY**

The researcher utilizes PuTTY for communication with the HPS Serial UART. PuTTY is a free and open-source terminal emulator, serial console and network file transfer application. It supports several network protocols, including SCP, SSH, Telnet, rlogin, and raw socket connection. The name "PuTTY" has no definitive meaning, though "tty" is the name for a terminal in the UNIX tradition, usually held to be short for Teletype. [40]

**1.7.2.2.8 Others**

There are many more software tools and utilities being used to develop this system. They are documented in APPENDIX I for reference.